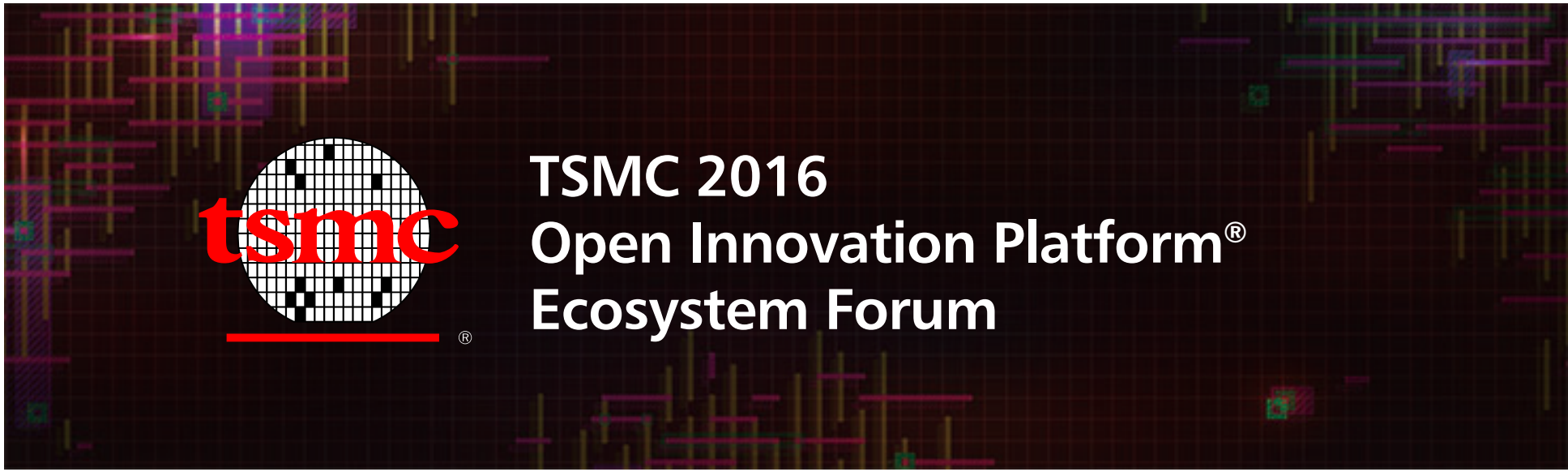
Timing Methodology for BEOL Variation

Qualcomm



ABSTRACT

At sub-16nm nodes, back end of line (BEOL) layers have become major sources of variation. Traditional timing methodology uses corner model, in which all BEOL layers are skewed to the worst-case condition (e.g., all BEOL layers have the worst parasitic capacitance). However, such a BEOL condition can be pessimistic because the probability of having all BEOL layers skew towards the worst-case condition simultaneously is extremely small. In this paper, we present a signoff methodology with tightened BEOL corners to recover the pessimism incurred by the conventional BEOL corners. This approach is based on the observation that most timing-critical paths use different BEOL layers. When the variation of BEOL layers are not fully correlated, the BEOL-induced timing variation is much smaller due to averaging of random variations. On the other hand, we also observe that a corner-based approach can be optimistic depending on wire distribution (e.g., when the launch and capture paths is dominated by different layers).